TITLE OF THE INVENTION

PLASMA DISPLAY PANEL AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to plasma display panels which are employed as an image display device for use with information terminal devices, personal computers, televisions or the like. More particularly, the present invention relates to a plasma display panel and its fabrication method which make it possible to provide a higher peak intensity and less maximum power consumption for a plasma display panel, having a large capacity and a high resolution, than prior-art panels and methods.

DESCRIPTION OF THE RELATED ART

Plasma display panels have such advantages that they have a simple construction, facilitates the provision of a large screen, and can employ inexpensive glass materials, which are widely used for glass windows or the like, as substrates for constituting the display panel.

A plasma display panel employs two transparent insulating substrates formed of such a glass material, each transparent insulating substrate having electrodes and ribs formed thereon to define pixel cells or display units. To complete the panel, these two transparent insulating substrates, having these structures formed thereon, are disposed in parallel spaced relation to define a gap therebetween in which a discharge gas is sealed. Typically, the rib is about 0.1mm in height and the transparent

insulating substrate is about 3mm in thickness, thereby making it possible to provide extremely thin and lightweight display devices.

Accordingly, by making use of such features, the plasma display panel has been being used in a display device for personal computers or office work stations, which have found widespread use in recent years, or for large-screen wall-hung televisions which have strong potential for further development.

The plasma display panel is largely classified into DC and AC types depending on the difference in panel structures. The plasma display panel with the electrodes being directly exposed to a discharge gas is referred to as the DC type because a DC current continues to flow once a discharge has occurred. On the other hand, the AC type with an insulating layer being interposed in between the electrodes and the discharge gas allows a pulse current to flow for a short period of time about 1μs after the application of a voltage and then converge. The flow of current is restricted by the electrostatic capacitance of the insulating layer. The insulating layer acts as a capacitor so that applied AC pulses cause repetitive pulses of light emission to occur for display purposes. This is why the AC type is called by that name.

Although the DC type has a simple structure, the electrodes are directly exposed to discharge environments and therefore wear out in a shorter period of time, thereby making it difficult to provide the DC type with long life.

In contrast, the AC type requires additional time, effort, and cost to form the insulating layer, however, the electrodes are covered with the insulating layer, thereby providing the AC type with long life. In addition, the AC type can readily implement the function referred to as a memory function, which enables highly bright light emission, and accordingly has been developed in recent years.

The present invention relates to this AC memory-type plasma display panel. Now, the configuration and then the method of the AC memory-type plasma display panel will be explained below.

First, the configuration of the AC memory-type plasma display panel is described. Figs. 1 to 3 are views illustrating an AC memory-type plasma display panel disclosed in Japanese Patent Laid-Open Publication No. Hei 6-12026 and having an electrode structure which is generally called a plane discharge type. Fig. 1 is a plan view, Fig. 2 is a cross-sectional view taken along line T-T of Fig. 1, and Fig. 3 is a cross-sectional view taken along line U-U of Fig. 1.

As shown in Fig. 2, this plasma display panel has first and second insulating substrates 11 and 12 which are transparent, 3mm in thickness, formed of soda glass, and disposed in parallel spaced relation to each other to allow light emission to pass therethrough for display purposes. In between the first insulating substrate 11 and the second insulating substrate 12, provided as basic constituents are the structures for the plasma display panel and sealed is a

discharge gas.

On the surface of the first insulating substrate 11 opposite to the second insulating substrate 12, a plurality of sustain electrodes 13a formed of transparent NESA film and a plurality of scan electrodes 13b also formed of transparent NESA film are disposed alternately in parallel to each other. In addition, a bus electrode 13c formed of silver thick film is disposed on top of each sustain electrode 13a and each scan electrode 13b to be in contact therewith, thereby making it possible to supply sufficient current to the sustain electrode 13a and the scan electrode 13b. These sustain electrode 13a, the scan electrode 13b, and the bus electrode 13c are formed to extend in the direction of horizontal rows in Fig. 1. Furthermore, these sustain electrode 13a, the scan electrode 13b, and the bus electrode 13c, are covered with an insulating layer 18a formed of thick transparent glaze film, and on top of the insulating layer 18a, a protective layer 19 of MgO having a thickness of 1 μm for protecting the insulating layer 18a from discharges is formed.

Incidentally, the sustain electrode 13a and the scan electrode 13b are generally referred to as a display electrode portion which plays a major role in emitting light for display purposes. In addition, the bus electrode 13c is to supply current to the display electrode portion. Likewise, the wiring portion for supplying current is often referred to as the bus electrode. In this context, the bus electrode 13c is sometimes referred to as the bus electrode

portion.

The electrode portion composed of the display electrode portion and the bus electrode portion is formed on the same surface of the glass substrate to provide an electrode constituting portion for causing plane discharges, and thus the display electrode portion and the bus electrode portion are generally referred to as the plane discharge electrode. For example, the plane discharge electrode on the side of the sustain electrode has the sustain electrode 13a as the display electrode portion and the bus electrode 13c on the sustain electrode 13a as the bus electrode.

Now, on the second insulating substrate 12, there are formed a plurality of column electrodes 14 of thick silver film to extend in the direction of horizontal rows in Fig. 1. The column electrode 14 and the second insulating substrate 12 are covered with a thick insulating layer 18b. In between the insulating layer 18b and the insulating layer 18a, ribs 16 of thick film are formed to provide spaces for the discharge gas and define pixel cells 20. Furthermore, a discharge gas is sealed in the discharge gas spaces 15 defined by the rib 16, and on the insulating layer 18b in each discharge gas space 15, there is provided a phosphor 17 made of Zn_2SiO_4:Mn for converting UV light produced by discharges in the discharge gas into visible light.

As described above, the two insulating substrates 11 and 12, each having respective structures formed thereon, are disposed in parallel spaced relation to each other to define a gap therebetween which acts as the discharge gas

space 15. The discharge gas space 15 is filled, at a total pressure of 66.5kPa, with a discharge gas of a gas mixture such as He and Ne mixed at a ratio of seven to three and added by 3% of Xe.

Referring to Fig. 1, the ribs 16 extending horizontally and vertically (in the directions of rows and columns) define discharge cells, which in turn act as pixel cells 20. In Fig. 4, a pixel cell is denoted by aij at the point of an intersection of a scan electrode Si (i=1, 2, …, m) and a column electrode Dj (j=1, 2, …, n). The phosphor 17 of Fig. 2 can be provided with three colors of red, green, and blue at each pixel cell, thereby providing a plasma display panel which enables full-color display. The display of this plasma display panel can be viewed from either side, that is, in the direction going upwards from the first insulating substrate 11 of Fig. 2 (in the direction of the upper surface) or in the direction going downwards from the second insulating substrate 12 (in the direction of the lower surface). For the plasma display panel shown in Figs. 1 to 3, it is preferable to view the display panel in the direction of the upper surface, which allows the light emitting portion at the phosphor 17 to be directly viewed and thereby provide higher intensity.

Incidentally, the insulating substrate on the side for viewing the display (the first insulating substrate 11 in this case) may be called the front substrate, while the other insulating substrate (the second insulating substrate 12 in this case) may be called the rear substrate. In

addition, in Fig. 1, the longitudinal direction of the bus electrode 13c is simply referred to as the row direction, while the longitudinal direction of the column electrode 14 is referred to as the column direction. Furthermore, since the plasma display panel often employs the column direction as the vertical direction, the column direction is assumed to be the vertical direction and the row direction as the horizontal direction for explanatory purposes. However, this is assumed merely for convenience and thus the column direction may be employed as the horizontal direction in practical uses.

Fig. 4 is a plan view illustrating only the arrangement of electrodes of the plasma display panel. Referring to Fig. 4, reference numeral 10 designates a plasma display panel; 21 designates a seal portion where the first insulating substrate 11 and the second insulating substrate 12 are disposed in parallel spaced relation to each other to define a gap therebetween in which a discharge gas is hermetically sealed; C1, C2, …, Cm designate the sustain electrodes 13a; S1, S2, …, Sm designate the scan electrodes 13b; and D1, D2, …, Dn-1, Dn designate the column electrodes 14. For example, a VGA-type actual plasma display panel has 480 pixel display units in the vertical direction and 640 pixel display units in the horizontal direction, where one pixel display unit consists of three pixel cells of R, G, and B. The VGA-type panel has 480 scan electrodes 13b (S1, S2, …, Sm) corresponding to the 480 pixel display units in the vertical direction, 480 sustain

electrodes 13a (C1, C2, …, Cm), and 1920 (=640×3) column electrodes 14 (D1, D2, …, Dn-1, Dn), which result from the 640 pixel display units, each being divided into three colors in the horizontal direction. Each pixel cell pitch is 0.35mm between the column electrodes 14 and 1.05mm between the scan electrodes 13b. The distance between the scan electrode 13b and the sustain electrode 13a, disposed parallel to each other, is 0.14mm.

Now, described below is a method for performing gray-scale display operation using the plasma display panel configured as described above. For the plasma display panel, unlike other types of display devices, it is difficult to change the level of applied voltages to thereby perform gray-scale display operation at a high intensity, and accordingly the number of times of light emission is controlled in general to perform gray-scale display operation. Particularly, to perform gray-scale display operation at a high intensity, employed is the sub-field method to be described below.

Fig. 5 is an explanatory view illustrating the drive sequence in accordance with the sub-field method. In Fig. 5, the horizontal axis represents the time and the vertical axis represents the scan electrode. A screenful of image is sent during the duration of one field. The duration of one field is often set to within the range of about 1/50 to 1/75 seconds depending on the computer or the broadcasting system.

As shown in Fig. 5, for gray-scale image display operation in the plasma display panel, one field is divided

into k sub-fields (k=6 sub-fields, or SF1 to SF6, in the case of Fig. 5). As will be described referring to Fig. 6, each sub-field is made up of a write cycle for writing display data with a preliminary discharge pulse 36, a preliminary discharge erase pulse 37, a scan pulse 33, a data pulse 34 or the like, and a sustain cycle for sustaining light emission for display purposes. Incidentally, in the write cycle, the preliminary discharge pulse and the preliminary discharge erase pulse may be omitted.

The luminous intensity of each pixel cell is controlled in accordance with the following equation 1 by assigning a weight of 2n to the number of times of light emission for sustain discharge at each pixel cell in each sub-field.

(Equation 1)

$$\text{Intensity} = L\,1 \times \sum_{n=1}^{k} 2^{(n-1)} \times a_n$$

where n is the sub-field number, being one (1) for the sub-field of the lowest intensity and k for the sub-field of the highest intensity; L1 is the intensity of the sub-field providing the lowest intensity; and a_n is a variable taking on a value of one or zero, being a value of one when the pixel cell emits light in the nth sub-field while zero when no light is emitted therefrom. Since different levels of luminous intensity are provided at each of the sub-fields, brightness can be controlled by selecting the "on" or "off"

state of each sub-field.

Since Fig. 5 shows the case of k=6, by color display operation with the red, green, and blue color pixel cells being grouped in one set, 64 ($2^k= 2^6$) levels of gray scale can be expressed with the colors. It is possible to display 64^3= 262,144 colors (including black). For k=1 or one field = one sub-field, the colors allow two levels ("on" or "off") of gray scale to be displayed. This allows 2^3= 8 colors (including black) to be displayed.

Fig. 6 is a view illustrating an example of drive voltage waveforms and a light emission waveform in the plasma display panel shown in Figs. 1 to 4. A waveform (A) represents a voltage waveform to be applied to the sustain electrodes 13a (C1, C2, …, Cm); a waveform (B) represents a voltage waveform to be applied to the scan electrode 13b (S1); a waveform (C) represents a voltage waveform to be applied to the scan electrode 13b (S2); a waveform (D) represents a voltage waveform to be applied to the scan electrode 13b (Sm); a waveform (E) represents a voltage waveform to be applied to the column electrode 14 (D1); a waveform (F) represents a voltage waveform to be applied to the column electrode 14 (D2); and a waveform (G) represents a light emission waveform of the pixel cell 20 (a11). The pulses having a diagonal line in the waveforms (E) and (F) indicate that the presence or absence of the pulses is determined in accordance with the presence or absence of data to be written. Fig. 6 shows the data voltage waveforms employed when data is written to the pixel cell 20 (a11,

a22). The figure also shows that display operation is performed at the pixel cells in the third and subsequent rows depending on the presence or absence of data.

A sustain pulse 31 and a preliminary discharge pulse 36 are applied to the sustain electrodes 13a (C1, C2, …, Cm). On the other hand, a sustain pulse 32, an erase pulse 35, and the preliminary discharge erase pulse 37 are applied successively in common to the scan electrodes 13b (S1, S2, …, Sm) in addition to the scan pulse 33 which is applied to each of the scan electrodes 13b (S1, S2, …, Sm) with independent timing. When light emission data is available, the data pulse 34 is applied to each of the column electrodes Dj (j=1, 2, …, n) in phase with the scan pulse 33. In the plasma display panel configured as shown in Figs. 1 to 4, the erase pulse 35 first erases the discharge in the pixel cell that has emitted light in the immediately previous sub-field. Then, the preliminary discharge pulse 36 causes a preliminary discharge to forcedly occur once in all pixel cells and then the preliminary discharge erase pulse 37 is allowed to erase the preliminary discharge. This allows the scan pulse 33 being subsequently applied to readily cause a write discharge.

After the preliminary discharge has been erased, application of the scan pulse 33 and the data pulse 34 to the scan electrode 13b and the column electrode 14 with the same timing to cause a write discharge will cause a discharge between the scan electrode and the column electrode at the same time for the write discharge. This is

referred to as the write sustain discharge. Subsequently, the sustain discharge is maintained between the sustain electrode 13a and scan electrode 13b, adjacent to each other, by the sustain pulses 31 and 32. On the other hand, application of only the scan pulse 33 or only the data pulse 34 would cause neither a write discharge nor a subsequent sustain discharge to occur. Such a function is called the memory function. The luminous intensity is controlled at each of the sub-fields depending on the number of times of sustain discharge.

However, as can be seen from the cross-sectional view of Fig. 3, there is a drawback, in outputting the light emitted from the phosphor 17 upwards in Fig. 55, that the bus electrode 13c present above the phosphor 17 provides an insufficient optical output efficiency. Accordingly, there is a problem that this provides a low ratio of luminous intensity to the power input for light emission (hereinafter referred to as the luminous efficiency), resulting in an increased power consumption of a display device employing the plasma display panel.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a plasma display panel which can provide a high optical- output efficiency and high peak intensity and which can be driven with less maximum power consumption, and a method for fabricating the panel.

As a first aspect, the present invention provides an AC plane discharge plasma display panel having a fundamental

structure including a front substrate, a rear substrate, and a sealing portion for encapsulating the front substrate and the rear substrate at a peripheral edge portion thereof to seal a discharge gas therebetween. The plasma display panel also includes column ribs and row ribs for defining pixel cells in a column direction and in a row direction, respectively, to thereby define the pixel cells in a matrix, and plane discharge electrodes constituted by a display electrode portion and a bus electrode portion. The plasma display panel is characterized in that at least part of the display electrode portion of the plane discharge electrodes has a notched portion or a cut-away portion between pixel cells adjacent to each other in the row direction; a sustain electrode and a scan electrode, paired as plane discharge electrodes, are placed in one pixel cell; and for neighboring pixel cells arranged in the column direction, sustain electrodes and scan electrodes are disposed to allow respective sustain electrodes and scan electrodes to be adjacent to each other between neighboring pixel cells. Furthermore, as a second aspect, there is provided the plasma display panel having the aforementioned fundamental structure according to the first aspect, characterized in that neighboring sustain electrodes or sustain-side bus electrodes for neighboring pixel cells arranged in the column direction are electrically connected to each other in the panel.

Furthermore, as a third aspect, there is provided the plasma display panel having the aforementioned fundamental

structure according to the first aspect, characterized in that neighboring scan electrodes or scan-side bus electrodes for neighboring pixel cells arranged in the column direction are electrically connected to each other in the panel.

Furthermore, as a fourth aspect, there is provided a method for fabricating the plasma display panel set forth in the aforementioned first to third aspect, characterized by including the steps of encapsulating the rear substrate and the front substrate in a vacuum, and sealing a discharge gas in the panel continually thereafter without exposing the interior of the panel to the atmosphere.

Furthermore, as a fifth aspect, there is provided the plasma display panel set forth in the aforementioned first to third aspect, characterized in that lattice-shaped ribs are formed on the rear substrate.

Furthermore, as a sixth aspect, there is provided the plasma display panel set forth in the aforementioned fifth aspect, characterized in that a gap for allowing a discharge gas to pass therethrough is provided between the top of the lattice-shaped rib and the front substrate.

Furthermore, as a seventh aspect, there is provided the plasma display panel set forth in the aforementioned sixth aspect, characterized in that projected portions are provided on intersections of lattice-shaped ribs of the front substrate or the rear substrate, the intersections corresponding to those of lattice-shaped ribs of the rear substrate.

Furthermore, as an eighth aspect, there is provided

the plasma display panel set forth in the aforementioned seventh aspect, characterized in that the projected portions define scan-side bus electrodes and sustain-side bus electrodes or scan electrodes and sustain electrodes between pixel cells adjacent to each other in the row direction.

Furthermore, as a ninth aspect, there is provided the plasma display panel set forth in the aforementioned sixth aspect, characterized in that recessed portions are provided on intersections of lattice-shaped ribs of the front substrate or the rear substrate, the intersections corresponding to those of lattice-shaped ribs of the rear substrate.

Furthermore, as a tenth aspect, there is provided the plasma display panel set forth in the aforementioned ninth aspect, characterized in that rib portions other than the recessed portions define at least scan electrodes and sustain electrodes between pixel cells adjacent to each other in the column direction.

Furthermore, as an eleventh aspect, there is provided the plasma display panel set forth in the aforementioned sixth aspect, characterized in that horizontal barrier walls having a thickness of 2 to 50 μm between pixel cells are formed in parallel to bus electrodes.

Furthermore, as a twelfth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh aspect, characterized in that the horizontal barrier wall is formed of a material having a dielectric constant lower than that of the insulating layer.

Furthermore, as a thirteenth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh aspect, characterized in that the horizontal barrier wall is placed only on one of the sustain electrodes or the scan electrodes between pixel cells extending in the longitudinal column direction.

Furthermore, as a fourteenth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh aspect, characterized in that the horizontal barrier walls on the sustain electrode and the scan electrode have different widths.

Furthermore, as a fifteenth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh to fourteenth aspect, characterized in that an extended portion is formed orthogonal to the longitudinal direction of the horizontal barrier wall, and the extended portion is disposed between pixel cells adjacent to each other in the longitudinal row direction.

Furthermore, as a sixteenth aspect, there is provided the plasma display panel set forth in the aforementioned sixth aspect, characterized in that lattice-shaped ribs are formed on the rear substrate, and a rib portion extending in the longitudinal row direction for defining pixel cells is higher than a rib portion extending in the longitudinal column direction for defining pixel cells.

Furthermore, as a seventeenth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh aspect, characterized in that a bus

electrode constituting the plane discharge electrode does not overlap the horizontal barrier wall but overlaps the rib.

Furthermore, as an eighteenth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh aspect, characterized in that a bus electrode constituting the plane discharge electrode does not overlap the rib but overlaps the horizontal barrier.

Furthermore, as a nineteenth aspect, there is provided the plasma display panel set forth in the aforementioned eleventh aspect, characterized in that a bus electrode constituting the plane discharge electrode is located so as to overlap the horizontal barrier wall and the rib.

Furthermore, as a twentieth aspect, there is provided the plasma display panel set forth in the aforementioned sixth aspect, characterized in that the bus electrode has a thickness of 10 to 50μm, and the thickness of the bus electrode causes a raised portion of thickness 2 to 50μm to be formed on the surface of the insulating layer.

Furthermore, as a twenty-first aspect, there is provided the plasma display panel set forth in the aforementioned first, second, and fifth to twentieth aspect, characterized in that a metal electrode connects between the sustain electrodes.

Furthermore, as a twenty-second aspect, there is provided the plasma display panel set forth in the aforementioned first, second, and fifth to twentieth aspect, characterized in that a transparent electrode connects between the sustain electrodes.

Furthermore, as a twenty-third aspect, there is provided the plasma display panel set forth in the aforementioned first, second, and fifth to twentieth aspect, characterized in that the sustain electrodes are connected to each other to act as an integrated common bus electrode.

Furthermore, as a twenty-fourth aspect, there is provided the plasma display panel set forth in the aforementioned twenty-third aspect, characterized in that resistance of the common bus electrode is 1/3 to 1/12 of that of the scan-side bus electrode.

Furthermore, as a twenty-fifth aspect, there is provided the plasma display panel set forth in the aforementioned twenty-third aspect, characterized in that the bus electrode has a thickness of 10 to 50 μm, and the thickness of the bus electrode causes a raised portion of thickness 2 to 50 μm to be formed on the surface of the insulating layer.

Furthermore, as a twenty-sixth aspect, there is provided the plasma display panel set forth in the aforementioned first, third, and fifth to twentieth aspect, characterized in that a metal electrode connects between the scan electrodes.

Furthermore, as a twenty-seventh aspect, there is provided the plasma display panel set forth in the aforementioned first, third, and fifth to twentieth aspect, characterized in that a transparent electrode connects between the scan electrodes.

Furthermore, as a twenty-eighth aspect, there is

provided the plasma display panel set forth in the aforementioned first, third, and fifth to twentieth aspect, characterized in that the scan electrodes are connected to each other to act as an integrated common bus electrode.

Furthermore, as a twenty-ninth aspect, there is provided the plasma display panel set forth in the aforementioned twenty-eighth aspect, characterized in that resistance of the common bus electrode is 1/3 to 1/12 of that of the sustain-side bus electrode.

Furthermore, as a thirtieth aspect, there is provided the plasma display panel set forth in the aforementioned twenty-eighth aspect, characterized in that the bus electrode has a thickness of 10 to 50 μm, and the thickness of the bus electrode causes a raised portion of thickness 2 to 50 μm to be formed on the surface of the insulating layer.

Furthermore, as a thirty-first aspect, there is provided the plasma display panel set forth in the aforementioned first, second, and fifth to twenty-fifth aspect, characterized in that the distance between the neighboring scan electrodes or the neighboring scan-side bus electrodes on vertically neighboring pixel cells is 20 to 200 μm.

Furthermore, as a thirty-second aspect, there is provided the plasma display panel set forth in the aforementioned first, third, fifth to twentieth, and twenty-sixth to thirtieth aspect, characterized in that the distance between the neighboring sustain electrodes or the neighboring sustain-side bus electrodes on vertically

neighboring pixel cells is 20 to 200μm.

Furthermore, as a thirty-third aspect, there is provided the plasma display panel set forth in the aforementioned first and second aspect, characterized in that the scan electrodes of neighboring pixel cells overlap each other being electrically insulated.

Furthermore, as a thirty-fourth aspect, there is provided the plasma display panel set forth in the aforementioned first and third aspect, characterized in that the sustain electrodes of neighboring pixel cells overlap each other being electrically insulated.

Furthermore, as a thirty-fifth aspect, there is provided the plasma display panel set forth in the aforementioned first to third and fifth to thirty-fourth aspect, characterized in that a notched or cut-away end portion of a display electrode portion disposed in the row direction is spaced apart by 20 to 70μm from a head portion of a rib disposed in the column direction.

Furthermore, as a thirty-sixth aspect, there is provided the plasma display panel set forth in the aforementioned first and second aspect, characterized in that the sustain electrode has a portion, reduced in width, for connecting to the sustain-side bus electrode.

Furthermore, as a thirty-seventh aspect, there is provided the plasma display panel set forth in the aforementioned first to third and fifth to thirty-sixth aspect, characterized in that the plane discharge electrode is constructed so as to allow pixel cells disposed in the

longitudinal column direction to have centers of light emission at equal intervals.

Furthermore, as a thirty-eighth aspect, there is provided the plasma display panel set forth in the aforementioned first to third and fifth to thirty-seventh aspect, characterized in that a horizontal black stripe is disposed between plane discharge electrodes or in the row direction including the plane discharge electrode.

Furthermore, as a thirty-ninth aspect, there is provided the plasma display panel set forth in the aforementioned thirty-eighth aspect, characterized in that horizontal black stripes, all having the same width, are disposed at equal intervals in the column direction to be vertically symmetric with each other in each pixel cell.

Furthermore, as a fortieth aspect, there is provided the plasma display panel set forth in the aforementioned thirty-eighth aspect, characterized in that a horizontal black stripe, a horizontal stripe made up of a scan electrode having a black or gray display side, and a horizontal stripe made up of a black or gray common bus electrode have the same width and are disposed at equal intervals in the column direction.

Furthermore, as a forty-first aspect, there is provided the plasma display panel set forth in the aforementioned thirty-eighth aspect, characterized in that scan electrodes and sustain electrodes are formed on the substrate, and horizontal black stripes are formed on the scan electrode and the sustain electrode.

Furthermore, as a forty-second aspect, there is provided the plasma display panel set forth in the aforementioned forty-first aspect, characterized in that a hole or notch is formed on the horizontal black stripe to ensure electrical connection of the scan electrode or the sustain electrode to the bus electrode.

As described above, the plasma display panel according to the present invention can employ the prior-art driving method to improve the intensity, the luminous efficiency, and the voltage margin. In addition, the plasma display panel can reduce unnecessary power consumption on the bus electrode provided on the sustain electrode and the overall percentage of breaks in the sustain electrode to thereby provide improved fabrication yields. Accordingly, the plasma display panel provides great effects of reducing the power consumption of and improving the reliability of the display device employing the plasma display panel and greatly contributing to saving energy.

In addition, the present invention provides electrodes having a shape equivalent to comb-teeth, thereby making it possible to increase the luminous efficiency. Lattice-shaped ribs allow the electrodes between pixel cells to be closely spaced and thereby the effective opening portion of a pixel cell can be increased. This prevents the intensity from being reduced even when the comb-tooth-shaped electrodes are employed to increase the luminous efficiency. Furthermore, the sustain electrodes or the scan electrodes are connected to each other or shared between the pixel

cells, thereby making it possible to provide further increased effective opening portion. This in turn makes it possible to provide further improved intensity and luminous efficiency. Furthermore, it is possible to reduce the resistance of electrodes, increase the voltage margin, improve the fabrication yields of the electrodes in the panel, and reduce the power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view illustrating the configuration of an AC memory-type plasma display panel;

Fig. 2 is a cross-sectional view taken along line T-T of Fig. 1;

Fig. 3 is a cross-sectional view taken along line U-U of Fig. 1;

Fig. 4 is a schematic view illustrating the arrangement of electrodes of a prior-art plasma display panel;

Fig. 5 is an explanatory view illustrating the drive sequence in accordance with a sub-field method;

Fig. 6 is a view illustrating an example of drive voltage waveforms and a light emission waveform in a sub-field;

Fig. 7 is a plan view illustrating a plasma display panel according to a first embodiment of the present invention;

Fig. 8 is a cross-sectional view taken along line A-A of Fig. 7;

Fig. 9 is a cross-sectional view taken along line B-B

of Fig. 7;

Fig. 10 is a plan view illustrating a plasma display panel according to a second embodiment of the present invention, being different from the first embodiment in employing thin metal wirings for scan and sustain electrodes;

Fig. 11 is a cross-sectional view taken along line C-C of Fig. 10;

Fig. 12 is a cross-sectional view taken along line D-D of Fig. 10;

Fig. 13 is a plan view illustrating a plasma display panel according to a third embodiment of the present invention, being different from the first embodiment in employing meshed thin metal wirings for scan and sustain electrodes;

Fig. 14 is a schematic view illustrating a device to be used for the fabrication method according to the present invention;

Fig. 15 is a perspective view illustrating a plasma display panel, having a projected at each intersection of the ribs, according to a fourth embodiment of the present invention;

Fig. 16 is a perspective view illustrating a plasma display panel according to a fifth embodiment of the present invention, in which a projection resides at each intersection of the ribs and the electrode portion for connecting between the right and left pixel cells is isolated by the rib projections;

Fig. 17 is a plan view also illustrating the fifth embodiment;

Fig. 18 is a perspective view illustrating a plasma display panel, having a recess at each intersection of the ribs, according to a sixth embodiment of the present invention;

Fig. 19 is a plan view illustrating a plasma display panel according to a seventh embodiment of the present invention in which the scan electrode, the sustain electrode, and the bus electrode of a pixel cell are separated from those of a neighboring pixel cell by the rib portion excluding the recesses residing at the intersections of the lattice rib;

Fig. 20 is a plan view illustrating a plasma display panel, having horizontal barrier walls, according to an eighth embodiment of the present invention;

Fig. 21 is a cross-sectional view taken along line F-F of Fig. 20;

Fig. 22 is a cross-sectional view taken along line G-G of Fig. 20;

Fig. 23 is a plan view illustrating a plasma display panel according to a ninth embodiment of the present invention in which a horizontal barrier wall is disposed only in between neighboring sustain electrodes or neighboring scan electrodes;

Fig. 24 is a plan view illustrating a plasma display panel according to a tenth embodiment of the present invention in which a horizontal barrier wall disposed in

between sustain electrodes is different in width from one disposed in between scan electrodes;

Fig. 25 is a plan view illustrating a plasma display panel according to an eleventh embodiment of the present invention;

Fig. 26 is a perspective view illustrating a plasma display panel according to a twelfth embodiment of the present invention;

Fig. 27 is a cross-sectional view illustrating a plasma display panel according to a thirteenth embodiment of the present invention;

Fig. 28 is a cross-sectional view illustrating a plasma display panel according to a fourteenth embodiment of the present invention;

Fig. 29 is a cross-sectional view illustrating a plasma display panel according to a fifteenth embodiment of the present invention;

Fig. 30 is a plan view illustrating a plasma display panel according to a sixteenth embodiment of the present invention;

Fig. 31 is a cross-sectional view taken along line H-H of Fig. 30;

Fig. 32 is a cross-sectional view taken along line I-I of Fig. 30;

Fig. 33 is a plan view illustrating a plasma display panel according to a seventeenth embodiment of the present invention;

Fig. 34 is a plan view illustrating a plasma display

panel according to an eighteenth embodiment of the present invention;

Fig. 35 is a cross-sectional view taken along line J-J of Fig. 34;

Fig. 36 is a cross-sectional view taken along line K-K of Fig. 34;

Fig. 37 is a cross-sectional view illustrating a plasma display panel according to a nineteenth embodiment of the present invention;

Fig. 38 is a cross-sectional view illustrating a plasma display panel according to a twentieth embodiment of the present invention;

Fig. 39 is a plan view illustrating a plasma display panel according to a twenty-first embodiment of the present invention;

Fig. 40 is a plan view illustrating a plasma display panel according to a twenty-second embodiment of the present invention;

Fig. 41 is a plan view illustrating the arrangement of pixel cells according to the eighth embodiment of the present invention;

Fig. 42 is a plan view illustrating a plasma display panel according to a twenty-third embodiment of the present invention;

Fig. 43 is a cross-sectional view taken along line L-L of Fig. 42;

Fig. 44 is a cross-sectional view taken along line M-M of Fig. 42;

Fig. 45 is a plan view illustrating a plasma display panel according to a twenty-fourth embodiment of the present invention;

Fig. 46 is a cross-sectional view taken along line N-N of Fig. 45;

Fig. 47 is a cross-sectional view taken along line O-O of Fig. 46;

Fig. 48 is a plan view illustrating a plasma display panel according to a twenty-fifth embodiment of the present invention;

Fig. 49 is a cross-sectional view taken along line P-P of Fig. 48;

Fig. 50 is a cross-sectional view taken along line Q-Q of Fig. 48;

Fig. 51 is a plan view illustrating a plasma display panel according to a twenty-sixth embodiment of the present invention;

Fig. 52 is a cross-sectional view taken along line R-R of Fig. 51;

Fig. 53 is a cross-sectional view taken along line S-S of Fig. 51;

Fig. 54 is a plan view illustrating a modified example of the twenty-sixth embodiment;

Fig. 55 is a schematic view of the arrangement of electrodes of an AC memory-type plane discharge plasma display panel, illustrating the connections of the scan electrodes and the sustain electrodes, which are interchanged to be driven using the panel configured

according to the present invention;

Fig. 56 is a cross-sectional view taken along a column electrode of Fig. 55;

Fig. 57 is a timing chart illustrating a drive method in accordance with the sub-field method; and

Figs. 58A to 58D are schematic views illustrating the state of wall charges inside the pixel cells of the panel shown in cross section in Fig. 56.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Now, a plasma display panel and its fabrication method according to the present invention will be explained below in more detail with reference to the accompanying drawings in accordance with the embodiments.

First embodiment

Fig. 7 is a plan view illustrating a plasma display panel according to a first embodiment of the present invention, Fig. 8 is a cross-sectional view taken along line A-A of Fig. 7, and Fig. 9 is a cross-sectional view taken along line B-B of Fig. 7. As shown in Fig. 8, the plasma display panel according to this embodiment has first and second insulating substrates 11 and 12 which are to serve as substrates, 3mm in thickness, and formed of soda glass. On the surface of the first insulating substrate 11 opposite to the second insulating substrate 12 (the surface behind the display surface), there reside sustain electrodes 13a and scan electrodes 13b, which are rectangular in shape and formed of transparent NESA film or ITO. The sustain-side

bus electrodes 13d and the scan-side bus electrodes 13e are disposed in parallel to each other and formed to extend in the row direction of Fig. 7. The sustain-side bus electrode 13d and the scan-side bus electrode 13e are in contact with the sustain electrode 13a and the scan electrode 13b, respectively, and are formed of silver thick film having a thickness of 1 to 9 μm to supply sufficient current to the sustain electrode 13a and the scan electrode 13b, which have high resistance. The sustain electrode 13a, the scan electrode 13b, the sustain-side bus electrode 13d, and the scan-side bus electrode 13e are covered with an insulating layer 18a which is formed of thick transparent glaze and has a thickness of 15 to 60 μm, and on top of the insulating layer 18a, a protective layer 19 of MgO having a thickness of 1 μm is formed for protecting the insulating layer 18a from discharges.

On the surface of the second insulating substrate 12 opposite to the first insulating substrate 11, a plurality of column electrodes 14 of thick silver film, having a thickness of 0.5 to 10 μm, are disposed in parallel to each other so as to extend in the row direction. In addition, an insulating layer 18b of thick film having a thickness of 5 to 40 μm is formed so as to cover the column electrode 14 and the inner surface of the second insulating substrate 12. Furthermore, formed on the insulating layer 18b are lattice-shaped ribs 16 of thick film having a thickness of 80 to 150 μm to provide discharge gas spaces 15 and define pixel cells 20, and a phosphor 17 is formed to cover the

insulating layer 18b and the sides of the rib 16 inside the pixel cell 20. The phosphor 17 is formed of Zn_2SiO_4:Mn, for converting UV light produced by discharges in the discharge gas into visible light. The first and second insulating substrates 11 and 12, each having the aforementioned respective constituents formed thereon, are disposed in parallel spaced relation to each other to define the discharge gas space 15, which is filled, at a total pressure of 66.5kPa, with a gas mixture of He and Ne containing 4% of Xe. The lattice-shaped ribs 16 define the pixel cells 20.

In this embodiment, the scan electrode 13b to be powered by the scan-side bus electrode 13e extending in the row direction is separated corresponding to each pixel cell 20 and formed in a rectangular shape elongated in the row direction. On the other hand, the sustain electrode 13a to be powered by the sustain-side bus electrode 13d extending in the row direction is separated from the pixel cells 20 adjacent thereto in the row direction and formed in a rectangular shape elongated in the column direction. The sustain electrode 13a and the scan electrode 13b do not reside on the rib 16 between pixel cells 20 adjacent to each other in the row direction but reside at the center of each pixel cell 20 in the row direction. The sustain electrode 13a, one in number, is provided in common for pixel cells 20 adjacent to each other in the column direction, and formed across a rib 16 for defining the pair of pixel cells 20 adjacent to each other in the column direction. Thus, this embodiment is adapted to have the scan electrodes 13b and

the sustain electrodes 13a in a manner such that the scan, sustain, sustain, scan, scan, sustain, and sustain electrodes are repeatedly disposed in that order in the column direction. In addition, at the center of each pixel cell 20 in the column direction, the scan electrode 13b and the sustain electrode 13a are spaced apart from each other by a discharge gap 22. A pair of neighboring sustain-side bus electrodes 13d, which are in contact with a common sustain electrode 13a, are electrically coupled to each other.

The sustain electrodes 13a and the scan electrodes 13b form a display electrode portion, while the sustain-side bus electrodes 13d and the scan-side bus electrodes 13e form a bus electrode portion. In addition, the sustain electrode 13a and the sustain-side bus electrode 13d are the sustain-side plane discharge electrodes, while the scan electrode 13b and the scan-side bus electrode 13e are scan-side plane discharge electrodes.

For explanatory purposes, this embodiment employs an exemplary panel which can display a so-called XGA-type window for use in personal computers or the like. A monitor of the XGA type has 768 display units in the vertical direction and 1,024 display units in the horizontal direction. Accordingly, the plasma display panel has 768/2 = 384 sustain electrodes 13a in each column, 768 scan electrodes 13b in each column, and 1024×3 = 3,072 column electrodes 14.

The plasma display panel has color pixels arranged in

vertical stripes, and color pixels acting as one display unit consist of three primary color pixel cells arranged in three columns.

For example, the color pixel cells are arranged at the same 0.6mm intervals in the vertical and horizontal directions. The ratio of the vertical to the horizontal dimension of the color pixel cell can take on 9:16, thereby making it possible to support a wide window that is frequently used by televisions or the like to display moving pictures. Alternatively, with the vertical and horizontal pitches remaining unchanged, the number of color pixel cells can be changed to support a wide window. For example, vertical color pixel cells may be 768 in number and horizontal color pixel cells may be 1365 in number.

The discharge gap 22 between the scan electrode 13b and the sustain electrode 13a is 70 μm, and the either side of the scan electrode 13b and the sustain electrode 13a is spaced 30 μm apart from the rib. This serves to reduce discharges of low luminous efficiency from plane discharge electrodes near the rib, thereby making it possible to increase the luminous efficiency. This distance of separation, 20 to 70 μm, can provide an effect of increasing the luminous efficiency. A distance of separation less than 20 μm would not provide a distinct effect. Furthermore, a distance of separation 70 μm or more would cause the effect to be saturated and the intensity to be reduced as well. The distance of separation is preferably 30 to 50 μm.

The distance between the sustain-side bus electrodes

13d for neighboring pixel cells or between the scan-side bus electrodes 13e for neighboring pixel cells is 100μm. Distances 20μm or less would cause the neighboring electrodes to be easily short-circuited and the electrostatic capacitance between the electrodes to increase. Distances between the electrodes 200μm or more would cause the electrostatic capacitance to decrease but the area of an effective opening portion to also decrease as describe later, thereby unpreferably resulting in reduction in intensity. Accordingly, the distance between the sustain-side bus electrodes 13d for neighboring pixel cells or between the scan-side bus electrodes 13e for neighboring pixel cells is preferably 20 to 200μm, and more preferably 50 to 150μm in practice for mass production purposes.

For example, the bus electrodes 13d, 13e have a width of 70μm. For example, the distance between the bus electrodes of vertically adjacent pixel cells 20 is 70μm. The end portion of the transparent scan electrode 13b and the scan-side bus electrode 13e overlap each other, for example, by 40μm. For example, the pitch of the column electrodes 14 is 0.2mm.

In the plasma display panel configured as described above, the either side of the rectangular sustain electrode 13a and the rectangular scan electrode 13b is spaced apart from the rib 16 in the row direction, thereby making it possible to reduce discharges of low luminous efficiency from the plane discharge electrodes near the rib 16 and thus increase the luminous efficiency. That is, since the scan

electrode 13b and the sustain electrode 13a are spaced apart from the ribs 16 adjacent thereto in the row direction, the discharge at portions of low luminous efficiency near the rib 16 is prevented to increase the ratio of light emission from portions of high luminous efficiency, thereby making it possible to increase luminous intensity with respect to the amount of input power.

Furthermore, this embodiment allows the lattice-shaped ribs 16 to block and thereby suppress spurious discharges which occur between the sustain electrodes or the scan electrodes of pixel cells adjacent to each other in the column direction. This makes it possible to place the sustain-side bus electrode 13d and the scan-side bus electrode 13e in close proximity to the ribs 16 to which the either electrode resides in parallel. A portion within one pixel cell which emits light with high intensity is an opening portion (hereinafter referred to as an effective opening portion) residing between the sustain-side bus electrode 13d and the scan-side bus electrode 13e. As described above, placing both the sustain-side bus electrode 13d formed of Ag and the scan-side bus electrode 13e in close proximity to the rib 16 would make it possible to provide an enlarged opening portion for emitting light with high intensity in the pixel cell, thereby allowing the intensity and the luminous efficiency to increase. Accordingly, this can sufficiently compensate for a decrease in intensity caused by the sustain electrode 13a and the scan electrode 13b formed in a rectangular shape.

In this embodiment, the sustain electrode 13a is disposed across pixel cells 20 adjacent to each other in the column direction in orthogonal relation to the rib 16 that is parallel to the sustain-side bus electrode 13d. The transparent electrodes cannot be visually recognized and apparently remain unchanged when compared with conventional ones, and make it possible to connect between the sustain electrodes 13a of neighboring pixel cells. Thus, two neighboring sustain-side bus electrodes 13d are electrically coupled to each other, thereby making it possible to reduce the overall electrode resistance of the two neighboring sustain-side bus electrodes 13d, for example, substantially by one-half. This provides a reduction in voltage drop across the sustain-side bus electrode 13d and a reduced rate of reduction in the voltage applied to the sustain electrode 13a of each pixel cell. This provides a reduction in minimum voltage to be applied from outside during a light emission discharge and reduced spurious erases for discharging pixel cells, thereby providing more stabilized display operation. Incidentally, the maximum voltage remains unchanged which can be applied from outside without causing spurious discharges during a light emission discharge. This makes it possible to provide an increased operational voltage margin or the difference between the aforementioned maximum and minimum voltages. This is hereinafter referred to as an "increase in operational voltage margin".

Thus, it is made possible to set voltages with

sufficient allowance with respect to a decrease in the aforementioned maximum voltage and an increase in the aforementioned minimum voltage caused by long-term operation. This allows the longevity of the plasma display panel to increase which is affected by spurious discharges or spurious erases, thereby making it possible to significantly improve the long-term reliability of the display device employing the plasma display panel.

Furthermore, two neighboring sustain-side bus electrodes 13d are electrically coupled to each other. Thus, even when one of the sustain-side bus electrodes 13d is on the verge of a break, the other neighboring sustain-side bus electrode 13d supplies current, thereby making it possible to provide increased yield of fabrication for a break in the electrodes.

Incidentally, the drive waveform according to the first embodiment of the method for driving the plasma display panel of the present invention is the same as that of Fig. 6. This is because the scan electrode 13b remains independent at each of the pixel cells disposed orthogonal to the scan electrode, like in the prior-art panel. This makes it possible to employ the prior-art drive method as it is with the effective opening portion of the pixel cell being increased.

<u>Fabrication method</u>

Now, described below is a method for fabricating the aforementioned plasma display panel according to the first embodiment of the present invention. Explained first is a

method for encapsulating and evacuating the plasma display panel having the configuration according to the first embodiment shown in Figs. 7 to 9. In the plasma display panel shown in Figs. 7 to 9, there exist slight gaps due to projected and recessed portions on the upper surfaces of the ribs 16 and the protective layer 19; however, each of the pixel cells is generally sealed by means of the ribs 16. According to the prior-art method, the first insulating substrate 11 and the second insulating substrate 12 are affixed to each other at the seal portion 21 (see Fig. 4) (which is called the encapsulating step). Then, the plasma display panel is once evacuated to a vacuum through an exhaust hole provided inside the seal portion 21 on the second insulating substrate 12, and then filled with a discharge gas. Thus, by the prior-art method, it would take a considerably long time to evacuate the plasma display panel to a vacuum since each of the pixel cells is almost sealed.

In this regard, to overcome this drawback, this embodiment is adapted to carry out part of the encapsulating step in a vacuum and subsequently a gas is introduced into the plasma display panel. This makes it possible to reduce the considerably long time required by the prior-art method for evacuating the panel to a vacuum. This fabrication method is hereinafter referred to as the vacuum encapsulation.

Fig. 14 is a schematic view illustrating a device to be used for the vacuum encapsulation. Referring to Fig. 14,

an encapsulation chamber 40 is adapted to accommodate, evacuate to a vacuum, and introduce a discharge gas into a plasma display panel, being coupled to a vacuum pump 41 via a pipe 71a. In addition, a first insulating substrate 51 accommodated in the encapsulation chamber 40 is provided with a hole 70 for exhausting air and introducing a gas, and the hole 70 is coupled to a vacuum pump 42 via a pipe 71b that is inserted into the encapsulation chamber 40. The pipe 71a is provided with a valve 46, while the pipe 71b is provided with a valve 75. In addition, the pipe 71a and the pipe 71b are coupled to each other via a pipe 71c, and the pipe 71c is provided with a gas heating portion 44 for heating a gas. There are provided valves 73 and 47 on both sides of the gas heating portion 44, a pipe for connecting between the pipe 71a and the outside is provided with a valve 45, and a pipe for connecting between the pipe 71b and the outside is provided with the valve 74. A gas cylinder 43 for accommodating a discharge gas is coupled to the gas heating portion 44 via a pipe 71d, and the pipe 71d is provided with a valve 48. The first insulating substrate 51 is provided with constituent elements such as electrodes and then accommodated in the chamber 40, while a second insulating substrate 52 is provided with electrodes, the ribs 16 and the like, and then accommodated in the chamber 40. The seal portion 21 is placed along the peripheral edge portion of the second insulating substrate 52. Incidentally, the pipe 71b can be separated by means of a connecting portion 72.

Now, the vacuum encapsulation process in the fabrication method according to this embodiment is explained step by step.

Step 1: First, the processed first insulating substrate 51 and the processed second insulating substrate 52 are inserted into the encapsulation chamber 40. With this arrangement, the seal portion 21 formed of low-melting glass and having a height 1.5 times as high as that of the rib 16 provides a sufficient gap between the first insulating substrate 51 and the second insulating substrate 52. In addition, at this stage, the insulating substrates 51 and 52 are aligned with each other in advance for the subsequent encapsulation. All the valves 45 to 48 and 73 to 75 are closed. The vacuum pumps 41 and 42 are activated.

Step 2: Then, the valve 46 is once opened to evacuate the chamber 40 and then closed. In addition, the valve 75 is once opened to evacuate the chamber 40 and then closed. This provides a degree of vacuum less than the atmospheric pressure or 10Pa or greater in the encapsulation chamber 40, preferably a degree of vacuum 1kPa to 50kPa. These degrees of vacuum are provided to allow the insulating substrates 51 and 52 to be readily heated in a short period of time by the heat conduction of the gas in the encapsulation chamber.

Step 3: The encapsulation chamber 40 is heated by a heater or the like installed outside or inside the encapsulation chamber 40 to remove moisture or oil present on the insulating substrate 51 or the inner wall of the encapsulation chamber. In this case, the inside of the

encapsulation chamber 40 is heated up to about 250 to 360℃ or preferably up to about 300 to 360℃. The heating is to be carried out up to the maximum temperature at which the low-melting glass used for the seal portion 21 is not softened.

Step 4: After the insulating substrates 51 and 52 have been heated up to a desired temperature in step 3, the valve 46 is opened slowly to allow the inside of the encapsulation chamber 40 to be evacuated to a vacuum. The moisture and oil, which have evaporated inside the encapsulation chamber 40, are thereby eliminated. Under this condition, the low-melting glass of the seal portion 21 has not yet been softened, and the first insulating substrate 51 and the second insulating substrate 52 provide a sufficient gap therebetween, thereby making it possible to effectively remove the evaporated moisture and oil.

Step 5: The encapsulation chamber 40 is further heated up to a higher temperature from about 430 to 470℃. This causes the material of the seal portion 21 or the low-melting glass to be softened, thereby allowing the substrates 51 and 52 having been thoroughly evacuated to be bonded together.

Step 6: Now, the temperature of the encapsulation chamber 40 is lowered close to the room temperature. Alternatively, the temperature of the substrates 51 and 52, encapsulated by the heat conduction of a gas, may be lowered. In this case, the valve 46 is closed, the valve 48 is slightly opened once, and the discharge gas is introduced

into a gas heating portion 49. Then, after the valve 48 has been closed, the valve 47 is slightly opened, the discharge gas is introduced into the encapsulation chamber 40, and then the valve 47 is closed again. At this time, the pressure of the gas in the encapsulation chamber is about 1Pa to 1kPa. Thus, the temperature of the encapsulated substrates 51 and 52 is lowered as the temperature of the encapsulation chamber 40 becomes lowered. Incidentally, just before starting to lower the temperature of the encapsulation chamber 40, the valve 75 is opened to further evacuate the inside of the encapsulated substrates 51 and 52 to a vacuum.

Step 7: The valve 75 is closed when the temperature of the encapsulated substrates 51 and 52 has been lowered close to the room temperature. Then, the valve 48 and the valve 73 are opened to introduce the discharge gas from the gas cylinder 43 into the encapsulated substrates 51 and 52. After the discharge gas has been introduced into the encapsulated substrates 51 and 52, the valve 48 and the valve 73 are closed.

Step 8: The exhaust pipe 71b is heated at the portion of line E-E shown in Fig. 14, and the exhaust pipe 71b is closed to complete the encapsulated substrates 51 and 52 as a plasma display panel.

Through the steps described above, the plasma display panel, having almost sealed pixel cells, shown in the first embodiment can be easily encapsulated and provided with a discharge gas therein in a short period of time. That is,

the present invention allows the first insulating substrate 51 and the second insulating substrate 52 to be evacuated to a vacuum as a whole in the encapsulation chamber 40 and then heated, thereby bonding and affixing the substrates 51 and 52 to each other at the seal portion 21. Then, after the temperature of the substrates 51 and 52 has been lowered in the chamber 40, a discharge gas is introduced therein. Increasing the temperature upon encapsulation causes gases to come out of the surface of the glass substrates 51 and 52 and the material of the seal portion 21. However, since the inside of the encapsulation chamber 40 and the gap between the substrates 51 and 52 have been evacuated to a vacuum upon encapsulation, these emitted gases can be exhausted quickly out of the panel. As described above, gases are thoroughly emitted from the surface of the glass substrates 51 and 52 and the sealing material, and a discharge gas is introduced into between the substrates 51 and 52 via the hole 70 after the temperature of the substrates 51 and 52 has been lowered. For this reason, this prevents the discharge gas from being contaminated and allows the discharge gas to be introduced into between the substrates with high service efficiency.

<u>Second embodiment</u>

Now, a plasma display panel according to a second embodiment of the present invention will be described with reference to Figs. 10 to 12. In Figs. 10 to 12, the same components as those of Figs. 7 to 9 are provided with the same reference symbols and will not be explained in detail

again. The first embodiment shown in Figs. 7 to 9 employs transparent electrodes as the sustain electrode 13a and the scan electrode 13b. However, the present invention is not limited thereto and can employ not only transparent electrodes but also thin metal electrodes.

Fig. 10 is a plan view illustrating a plasma display panel which employs thin metal wirings as the scan and sustain electrodes instead of the transparent electrodes of the first embodiment according to the first embodiment. Fig. 11 is a cross-sectional view taken along line C-C of Fig. 10 and Fig. 12 is a cross-sectional view taken along line D-D of Fig. 10. In Figs. 10 to 12, the same components as those of Figs. 7 to 9 are provided with the same reference symbols and will not be explained in detail again.

As shown in Figs. 10 to 12, this embodiment employs gate-shaped sustain electrodes 13a and scan electrodes 13b formed of metal. These electrodes can be formed through the same process as that for the sustain-side bus electrode 13d and the scan-side bus electrode 13e. These electrodes have a narrow width and therefore do not considerably block light emission. This lessens the need to employ transparent materials and the step of forming transparent electrodes can be omitted by employing metal electrodes as in this embodiment. This in turn makes it possible to reduce costs.

Incidentally, the metal electrode is not limited to the gate-shaped type and can employ various shapes such as a lattice-shaped or T-shaped type. Furthermore, the metal electrode can be formed in a fine mesh shape.

Third embodiment

Fig. 13 is a plan view illustrating a third embodiment of the present invention. This embodiment employs meshed metal wirings as the scan and sustain electrodes of the first embodiment. The sustain electrode 13a and the scan electrode 13b are formed in the shape of mesh.

Fourth embodiment

Now, a fourth embodiment of the present invention is described below.

Fig. 15 is a perspective view illustrating a second insulating substrate 12 of a plasma display panel according to a fourth embodiment of the present invention. In this embodiment, lattice-shaped ribs 16 are formed on top of the second insulating substrate 12, and rib projections 53 are formed at the intersection of the ribs 16. After the rib 16 has been formed by the sandblasting method, the screen printing method can be employed to directly print, dry, and bake the rib projection 53. To form the rib projection 53, a photosensitive paste can be printed on top of the ribs by employing the contact printing method other than the screen printing method. Then, the rib projection 53 is patterned, exposed, and developed using photo-masks in order to allow only the rib projection 53 to remain and to be baked. Furthermore, ribs having projected portions can be directly formed using a three-dimensional mold.

The plasma display panel according to the fourth embodiment of the present invention provides a flow path for a gas to be exhausted therethrough to a vacuum, thereby

making it possible to perform exhaustion easily by the same encapsulating and exhausting method as the prior-art method. Incidentally, in Fig. 15, for ease of understanding, components other than the ribs 16, the rib projections 53, and the second insulating substrate 12 are not illustrated. It is to be understood that the components other than the ribs 16, the rib projections 53, and the second insulating substrate 12 are the same as those of the first embodiment.

Fifth embodiment

Now, a fifth embodiment of the present invention is described below. Fig. 16 is a perspective view illustrating a second insulating substrate 12 of a plasma display panel according to the fifth embodiment of the present invention. Fig. 17 is a plan view illustrating the plasma display panel according to the fifth embodiment of the present invention. In this embodiment, rib projections 53 are formed to extend in either direction from the intersections of the lattice-shaped ribs 16 in parallel to the direction of the column electrodes. As shown in Fig. 17, this allows the scan-side bus electrode 13e and the sustain-side bus electrode 13d to be separated from each other between neighboring pixel cells. The method for fabricating the plasma display panel according to this embodiment is the same as that of the fourth embodiment.

Even with projections residing at the intersections of the lattice-shaped ribs, the rib projections 53 allow the scan-side bus electrode 13e and the sustain-side bus electrode 13d to be separated from each other between

neighboring pixel cells, thereby making it possible to prevent spurious light emission caused by currents flowing through the scan-side bus electrode 13e and the sustain-side bus electrode 13d between the neighboring pixel cells.

Incidentally, the rib projections 53 can be formed not on top of the ribs 16 as shown in Fig. 16 but on top of the insulating layer 18a of the first insulating substrate 11. Even in this case, the screen printing method, described in the third embodiment, can be employed to directly form the rib projections 53. Alternatively, such a method can also be employed in which the photosensitive paste, mentioned in the fourth embodiment, is printed by the contact printing method, and then patterned using photo-masks and baked.

<u>Sixth embodiment</u>

Now, a sixth embodiment of the present invention is described below. Fig. 18 is a perspective view illustrating the configuration of a plasma display panel according to the sixth embodiment of the present invention. In this embodiment, the lattice-shaped rib 16 is formed on top of the second insulating substrate 12, and rib recesses 54 are formed on the intersection of the ribs 16. This provides flow paths for a gas to be exhausted to a vacuum, thereby making it possible to easily perform exhaustion by the same encapsulating and exhausting method as the prior-art method. Incidentally, in Fig. 18, for the sake of simplification of illustration, components other than the ribs 16, the rib recesses 54, and the second insulating substrate 12 are not shown. The components other than the ribs 16, the rib

recesses 54, and the second insulating substrate 12 are the same as those of the first embodiment. In addition, it is possible to employ the fabrication methods described in the third and fourth embodiments for this embodiment.

The sixth embodiment provides an effect of facilitating vacuuming upon encapsulation. Furthermore, the central portion of each side of the ribs for defining pixel cells is separated by the ribs 16, thereby making it possible to reduce vertical and horizontal spurious light emission through the gaps communicating between pixel cells.

Seventh embodiment

Now, a seventh embodiment according to the present invention is described below. Fig. 19 is a plan view illustrating a plasma display panel according to the seventh embodiment of the present invention. In this embodiment, like the sixth embodiment shown in Fig. 18, the lattice-shaped rib 16 is formed on top of the second insulating substrate 12, and rib recesses 54 are formed on the intersection of the ribs 16. Additionally, in this embodiment, as in the embodiment shown in Fig. 7, there are formed the sustain electrode 13a, the scan electrode 13b, the sustain-side bus electrode 13d, and the scan-side bus electrode 13e. This embodiment also has the rib recesses 54 on top of the intersections of the ribs 16 to provide flow paths for a gas to be exhausted to a vacuum, thereby making it possible to easily perform exhaustion by the same encapsulating and exhausting method as the prior-art method. Incidentally, it is possible to fabricate the plasma display

panel according to this embodiment in the same manner as that of the third to the sixth embodiments.

Unlike the fifth embodiment, this embodiment allows the scan-side bus electrode 13e, the sustain-side bus electrode 13d, and the sustain electrode 13a to be separated between neighboring pixel cells by the rib portions other than the rib recesses 54 residing on the intersections of the lattice-shaped ribs.

This seventh embodiment provides an effect of facilitating vacuuming upon encapsulation. Furthermore, the central portion of each side of the ribs 16 for defining pixel cells separates the gap between pixel cells, also defining the scan electrode 13b, the sustain electrode 13a, and the bus electrode 13c between neighboring pixel cells. Thus, even with the rib recesses 54 residing on the intersections of the lattice-shaped ribs 16, it is possible to effectively prevent spurious light emission transmitting along the scan electrode 13b, the sustain electrode 13a, and the bus electrode 13c between the neighboring pixel cells.

Eighth embodiment

Now, an eighth embodiment according to the present invention is described below. Fig. 20 is a plan view illustrating a plasma display panel according to the eighth embodiment of the present invention. Fig. 21 is a cross-sectional view taken along line F-F of Fig. 20 and Fig. 22 is a cross-sectional view taken along line G-G of Fig. 20. The same components of Figs. 20 to 22 as those of Figs. 7 to 9 are provided with the same reference symbols and will not

be repeatedly explained in detail.

This eighth embodiment is different from the first embodiment in having horizontal barrier walls 23. In this embodiment, the horizontal barrier wall 23 is formed on top of the insulating layer 18a of the first insulating substrate 11. The horizontal barrier wall 23 has a height of 2 to 50μm and desirably 5 to 30μm. In addition, the horizontal barrier wall 23 is located between the sustain-side bus electrodes 13d and between the scan-side bus electrodes 13e.

It is possible to form the horizontal barrier wall 23, using a patterned screen, by employing the thick-film printing method to perform pattern printing directly on the insulating layer 18a and then by baking the horizontal barrier wall 23. Alternatively, a photosensitive paste can be printed on a plane by contact printing and dried, which is in turn radiated with UV light through masks, exposed, developed, dried, and then baked to form a pattern.

The horizontal barrier wall 23 can be formed of a transparent glass material. Alternatively, to increase contrast, the material may be mixed with a black material (such as cobalt oxide, ruthenium oxide, or iron oxide). Alternatively, to provide efficient reflections of light emitted from pixel cells, titanium oxide, zirconium oxide, alumina, silicon oxide, or the like) may be mixed with the material to form a white material. Alternatively, the display side (on the side of the first insulating substrate 11) may be formed in black to provide increased contrast,

whereas the pixel interior side may be formed in white to provide effective reflections of light generated inside pixel cells.

The horizontal barrier wall 23 provides an exhaustion path in the longitudinal direction of the scan-side bus electrode 13e. This makes it possible, without using the vacuum encapsulation described with reference to Fig. 14, to affix the first and second insulating substrates to each other, on each of which structures have been formed in an atmospheric environment in the same manner as that of the prior art, and then perform the evacuation of and introduction of a gas into the plasma display panel.

To eliminate unnecessary power consumption required for charging or discharging electrostatic capacitance by pulse voltages applied upon driving the plasma display panel, it is desirable that the electrostatic capacitance should be small between the scan-side bus electrodes 13e in neighboring pixel cells and between the sustain-side bus electrode 13d, the scan-side bus electrode 13e, and the column electrode 14. In this context, the material of the horizontal barrier wall 23 has desirably a low dielectric constant. It is possible to employ a zinc-oxide-based glass material (having a dielectric constant of about 8) instead of a lead-glass-based insulating material (having a dielectric constant of about 13) to reduce the dielectric constant, thereby reducing the power consumption of the plasma display panel.

The horizontal barrier wall 23 provides an exhaustion

path in the longitudinal direction of the scan-side bus electrode 13e. This makes it possible, without using the vacuum encapsulation described with reference to Fig. 14, to affix the first and second insulating substrates to each other, on each of which structures have been formed in an atmospheric environment in the same manner as that of the prior art, and then perform the evacuation of and introduction of a gas into the plasma display panel.

Furthermore, the reduction in dielectric constant of the horizontal barrier wall 23 results in a reduction in electrostatic capacitance between electrodes, thereby making it possible to prevent an increase in ineffective power consumption.

Ninth embodiment

Now, a ninth embodiment according to the present invention is described below. Fig. 23 is a plan view illustrating a plasma display panel according to the ninth embodiment of the present invention. As can be seen from Fig. 23, this embodiment provides the horizontal barrier wall 23 only between the sustain-side bus electrodes 13d. Spurious discharges often occur along the sustain electrode 13a connecting between vertical pixel cells 20. Thus, the horizontal barrier wall 23 provided between sustain-side bus electrodes 13d as in this embodiment obviates the need to always separate the scan-side bus electrodes 13e from each other by the horizontal barrier wall 23. The plasma display panel according to this embodiment can be fabricated by the same method as that of the eighth embodiment. The

configuration according to this embodiment can increase the exhaustion path in size, thereby reducing the time required for exhaustion.

Tenth embodiment

Now, a tenth embodiment according to the present invention is explained below. Fig. 24 is a plan view illustrating a plasma display panel according to the tenth embodiment of the present invention. As can be seen from Fig. 24, in this embodiment, the horizontal barrier wall 23 between scan-side bus electrodes 13e has a width narrower than that of the horizontal barrier wall 23 between sustain-side bus electrodes 13d. This makes the exhaustion path larger than that of the eighth embodiment shown in Fig. 20, thereby reducing the time required for exhaustion. Incidentally, the same fabrication method as that of the eighth embodiment can be applied to this embodiment.

Eleventh embodiment

Now, an eleventh embodiment according to the present invention is described below. Fig. 25 is a plan view illustrating a plasma display panel according to the eleventh embodiment of the present invention. As can be seen from Fig. 25, in this embodiment, the horizontal barrier wall 23 is provided with extensions 55 perpendicular to the longitudinal direction of the horizontal barrier wall 23, and disposed between pixel cells 20 across the sustain-side bus electrodes 13d and across the scan-side bus electrodes 13e. This allows the horizontal barrier wall 23 to provide an exhaustion path to reduce the time required

for exhaustion. Moreover, this allows the extension 55 to effectively prevent spurious light emission transmitting along the sustain-side bus electrode 13d and the scan-side bus electrode 13e between neighboring pixel cells 20. Incidentally, the same fabrication method as that of the eighth embodiment can be applied to this embodiment.

Twelfth embodiment

Now, a twelfth embodiment according to the present invention is described below. Fig. 26 is a perspective view illustrating a plasma display panel according to the twelfth embodiment of the present invention. Referring to Fig. 26, this embodiment is different from the first embodiment in having the horizontal barrier walls 23 on the ribs 16.

The horizontal barrier wall 23 has a height of 2 to 50 μm, desirably 5 to 30μm. In addition, the horizontal barrier wall 23 is located between the pixel cells corresponding to the sustain-side bus electrodes 13d adjacent to each other or between the pixel cells corresponding to the scan-side bus electrodes 13e, on the second insulating substrate 12.

The horizontal barrier wall 23 can be formed integrally with the ribs 16. Alternatively, it is possible to form the horizontal barrier wall 23, using a patterned screen, by employing the thick-film printing method to directly perform pattern printing on the ribs 16 having a uniformly formed height and then by baking the horizontal barrier wall 23. Alternatively, the horizontal barrier wall 23 can also be formed using a photosensitive paste in the

same manner as that of the fourth embodiment.

The horizontal barrier wall 23 can be formed of a transparent glass material. Alternatively, to increase contrast, the material may be mixed with a black material (such as cobalt oxide, ruthenium oxide, or iron oxide). Alternatively, to provide efficient reflections of light emitted from pixel cells, titanium oxide, zirconium oxide, alumina, silicon oxide, or the like) may be mixed with the material to form a white material.

Like the eighth embodiment, this embodiment allows the horizontal barrier wall 23 to provide an exhaustion path in the longitudinal direction of the scan-side bus electrode 13e. This makes it possible, without using the vacuum encapsulation described with reference to Fig. 14, to affix the first and second insulating substrates to each other, on each of which structures have been formed in an atmospheric environment in the same manner as that of the prior art, and then perform the evacuation of and introduction of a gas into the plasma display panel. Furthermore, this embodiment provides an advantage of simplifying the fabrication process since the ribs and the horizontal barrier walls are formed only on one insulating substrate.

Thirteenth embodiment

Now, a thirteenth embodiment according to the present invention is described below. Fig. 27 is a cross-sectional view illustrating a plasma display panel according to the thirteenth embodiment of the present invention. Like the plasma display panel according to the eighth embodiment

shown in Fig. 21, this embodiment employs the horizontal barrier wall 23. The rib 16 opposite to the horizontal barrier wall 23 has a width greater than that opposite to a pair of sustain-side bus electrodes 13d or scan-side bus electrodes 13e as shown in Fig. 27. This makes it possible to prevent discharges, occurring on the bus electrodes 13d, 13e and providing low optical output efficiency, and increase the luminous efficiency of pixel cells. In this case, without increasing the electrostatic capacitance established via the horizontal barrier wall 23 between the sustain-side bus electrode 13d and the scan-side bus electrode 13e, it is possible to increase the luminous efficiency of pixel cells while preventing discharges, occurring on the bus electrodes and providing low optical output efficiency.

That is, the ribs 16 located to overlap the bus electrodes 13d, 13e can prevent the light emission on the bus electrodes 13d, 13e, thereby making it possible to increase the luminous efficiency. This in turn makes it possible to increase intensity for the same light emission power. In other words, with the intensity remaining unchanged, the light emission power can be reduced.

<u>Fourteenth embodiment</u>

Now, a fourteenth embodiment according to the present invention is described below. Fig. 28 is a cross-sectional view illustrating a plasma display panel according to the fourteenth embodiment of the present invention. Like the eighth embodiment shown in Fig. 21, this embodiment also

employs the horizontal barrier wall 23. As shown in Fig. 28, the horizontal barrier wall 23 has a width extended to cover the bus electrodes 13d, 13e. This makes it possible to prevent discharges, occurring on the bus electrodes 13d, 13e and providing low optical output efficiency, and further increase the luminous efficiency of pixel cells.

This in turn makes it possible to increase intensity for the same light emission power. In other words, with the intensity remaining unchanged, the light emission power can be reduced. Furthermore, since the bus electrodes 13d, 13e do not overlap the ribs 16, the electrostatic capacitance between the scan electrode 13b or the sustain electrode 13a and the column electrode 14 is reduced.

Fifteenth embodiment

Now, a fifteenth embodiment according to the present invention is described below. Fig. 29 is a cross-sectional view illustrating a plasma display panel according to the fifteenth embodiment of the present invention. This embodiment employs the horizontal barrier wall 23 of the eighth embodiment shown in Fig. 21. In this embodiment, as shown in Fig. 29, the contact area between the rib 16 and the horizontal barrier wall 23 is increased to place the first priority on preventing damage to the rib when being subjected to vibration or shock. As shown in Fig. 29, the horizontal barrier wall 23 and the rib 16 opposite to the horizontal barrier wall 23 are extended in width to cover the bus electrodes 13d, 13e. In this case, it is possible to increase the luminous efficiency although the

electrostatic capacitance between the sustain-side bus electrode 13d and the scan-side bus electrode 13e and between the sustain-side and scan-side bus electrodes 13d, 13e and the column electrode 14 are increased.

The horizontal barrier wall 23 and the rib 16 located to overlap the bus electrodes 13d, 13e can prevent the light emission on the bus electrodes 13d, 13e, thereby making it possible to increase the luminous efficiency. White ribs 16 would reflect visible light from ribs, thereby making it possible to further increase the luminous efficiency. This increase in light emission in turn makes it possible to increase intensity for the same light emission power. In other words, with the intensity remaining unchanged, the light emission power can be reduced.

Incidentally, in the thirteenth to fifteenth embodiments, the sustain-side bus electrodes 13d and the scan-side bus electrodes 13e have the same thickness as that of the prior art ones (about 3 to 8 μm). However, in these embodiments, since the discharges on the sustain-side bus electrodes 13d and the scan-side bus electrodes 13e are substantially prevented, these bus electrodes 13d, 13e may be made greater in width than those of prior art. More specifically, with the bus electrodes 13d, 13e being increased in width up to about 10 to 25 μm, the insulating layer 18a (normally having a thickness of 20 to 40 μm) having a decreased thickness would cause an extremely large discharge, preventing the insulating layer 18a and the protective layer 19 from being subjected to an electrical

breakdown.

This makes it possible to reduce the electrode resistance of the sustain-side bus electrode 13d and the scan-side bus electrode 13e to about 1/2 to 1/5 of the conventional value. This also causes the voltage drop across the sustain-side bus electrode 13d and the scan-side bus electrode 13e to be made smaller than conventional value. This provides a reduced rate of reduction in the voltage applied to the sustain electrode 13a or the scan electrode 13b of each pixel cell. This provides a reduction in minimum voltage to be applied from outside during a light emission discharge and reduced spurious erases for discharging pixel cells, thereby providing more stabilized display operation. Incidentally, the maximum voltage remains unchanged which can be applied from outside without causing spurious discharges during a light emission discharge. This makes it possible to provide an increased operational voltage margin or the difference between the aforementioned maximum and minimum voltages.

Thus, it is made possible to set voltages with sufficient allowance with respect to a decrease in the aforementioned maximum voltage and an increase in the aforementioned minimum voltage caused by long-term operation. This allows the longevity of the plasma display panel to increase which is affected by spurious discharges or spurious erases, thereby making it possible to significantly improve the long-term reliability of the display device employing the plasma display panel.

Sixteenth embodiment

Now, a sixteenth embodiment according to the present invention is described below. Fig. 30 is a plan view illustrating a plasma display panel according to the sixteenth embodiment of the present invention. Fig. 31 is a cross-sectional view taken along line H-H of Fig. 30, and Fig. 32 is a cross-sectional view taken along line I-I of Fig. 30. As shown in Figs. 30 to 32, in this embodiment, the thickness of the sustain-side bus electrode 13d and the scan-side bus electrode 13e causes the surface of the insulating layer 18a to project by that thickness, thus creating bumps 64 on the insulating layer 18a.

As described above, to raise the sustain-side bus electrode 13d and the scan-side bus electrode 13e to cause the insulating layer 18a to be also raised, control may be exercised over the leveling property of the insulating layer paste upon being dried and the reflow property thereof upon being baked, by the material and adjustment of baking temperatures upon printing, drying, and baking the thick insulating layer 18a. For example, the amount of the thinner component of print paste is reduced to be less than usual and the maximum temperature of baking is also reduced by about 5 to 50℃, thereby making it possible to form the bump 64. Furthermore, it is also effective to reduce the maximum temperature of baking and the length of time periods of the maximum temperature and temperatures before and after the maximum temperature.

This embodiment with the configuration described above

can provide an effect equivalent to the horizontal barrier wall 23 without forming the horizontal barrier wall 23. This makes it possible to facilitate the fabrication process and provide a significant reduction in cost.

For example, the sustain-side bus electrode 13d and the scan-side bus electrode 13e have a thickness of 10 to 50 μm. Correspondingly, the bump 64 can have a height of 2 to 50μm at the portions having no underlying bus electrodes 13d, 13e. The bus electrodes 13d, 13e conventionally have a thickness of 1 to 9μm and about 5μm on average. In contrast, this embodiment provides the bus electrodes 13d, 13e with a thickness of 10 to 50μm. Thus, this embodiment provides a second effect that the resistance of the sustain-side bus electrode 13d and the scan-side bus electrode 13e can be reduced to 1/2 to 1/10 of the conventional average electrode resistance.

Furthermore, the sustain electrode 13a connects electrically two neighboring sustain-side bus electrodes 13d to each other. It is therefore possible to substantially reduce the overall electrode resistance of the two neighboring sustain-side bus electrodes 13d to 1/4 to 1/20 of the conventional value. This reduces the voltage drop across the sustain-side bus electrode 13d to be significantly less than that provided by the first embodiment. This makes it possible to reduce the rate of reduction, caused by the voltage drop across the sustain-side bus electrode 13d, in the voltage applied to the sustain electrode 13a of each pixel cell. This provides a

reduction in minimum voltage to be applied from outside during a light emission discharge and reduced spurious erases for discharging pixel cells, thereby providing more stabilized display operation. Incidentally, the maximum voltage remains unchanged which can be applied from outside without causing spurious discharges during a light emission discharge. This makes it possible to provide an increased operational voltage margin or the difference between the aforementioned maximum and minimum voltages.

Thus, it is made possible to set voltages with sufficient allowance with respect to a decrease in the aforementioned maximum voltage and an increase in the aforementioned minimum voltage caused by long-term operation. This allows the longevity of the plasma display panel to increase which is affected by spurious discharges or spurious erases, thereby making it possible to significantly improve the long-term reliability of the display device employing the plasma display panel.

Furthermore, two neighboring sustain-side bus electrodes 13d are electrically coupled to each other. Thus, even when one of the sustain-side bus electrodes 13d is on the verge of a break, the other neighboring sustain-side bus electrode 13d supplies current, thereby making it possible to provide increased yield of fabrication for a break in the electrodes. Incidentally, when thick bus electrodes 13d, 13e are employed as in this embodiment, it is possible to use a silver paste increased in volume by mixing the paste with a fine particle filler formed such as of alumina or

silica to avoid an increase in cost caused by the expensive silver paste.

Seventeenth embodiment

Now, a seventeenth embodiment according to the present invention is described below. Fig. 33 is a plan view illustrating a plasma display panel according to the seventeenth embodiment of the present invention. Referring to Fig. 33, connecting portions 56, formed of the same material as that of the sustain-side bus electrode 13d, connect the sustain-side bus electrodes 13d of neighboring pixel cells to each other.

This allows the connecting portion 56 to electrically connect two neighboring sustain-side bus electrodes 13d to each other, thereby making it possible to substantially reduce the overall electrode resistance of the two neighboring sustain-side bus electrodes 13d by one-half. This provides a reduction in voltage drop across the sustain-side bus electrode 13d and a reduced rate of reduction in the voltage applied to the sustain electrode 13a of each pixel cell. This provides a reduction in minimum voltage to be applied from outside during a light emission discharge and reduced spurious erases for discharging pixel cells, thereby providing further stabilized display operation. Incidentally, the maximum voltage remains unchanged which can be applied from outside without causing spurious discharges during a light emission discharge. This makes it possible to provide an increased operational voltage margin or the difference between the

aforementioned maximum and minimum voltages.

Thus, it is made possible to set voltages with sufficient allowance with respect to a decrease in the aforementioned maximum voltage and an increase in the aforementioned minimum voltage caused by long-term operation. This allows the longevity of the plasma display panel to increase which is affected by spurious discharges or spurious erases, thereby making it possible to significantly improve the long-term reliability of the display device employing the plasma display panel.

Furthermore, two neighboring sustain-side bus electrodes 13d are electrically coupled to each other. Thus, even when one of the sustain-side bus electrodes 13d is on the verge of a break, the other neighboring sustain-side bus electrode 13d supplies current, thereby making it possible to provide increased yield of fabrication for a break in the electrodes. This effect is greater than that provided by the first embodiment in which transparent electrodes, greater in resistance than the bus electrode by several orders of magnitude, between the bus electrodes.

Incidentally, referring to Fig. 33, the neighboring sustain-side bus electrodes 13d are connected to each by the connecting portion 56 and shared by the vertically neighboring pixel cells. However, apart from this, the sustain electrode 13a can also be made independent for each pixel cell, like the scan electrode 13b. Furthermore, since the sustain-side bus electrodes 13d are electrically connected to each other by the connecting portion 56, the

sustain electrode 13a can be made independent at each pixel cell.

Eighteenth embodiment

Now, an eighteenth embodiment according to the present invention is described below. Fig. 34 is a plan view illustrating a plasma display panel according to the eighteenth embodiment of the present invention. Fig. 35 is a cross-sectional view taken along line J-J of Fig. 34, and Fig. 36 is a cross-sectional view taken along line K-K of Fig. 34. This embodiment allows the sustain-side bus electrodes 13d of neighboring pixel cells to be perfectly shared and employed as a common bus electrode 57.

This allows the two neighboring sustain-side bus electrodes 13d to be electrically connected to each other to perfection. As described in the first embodiment, the non-shared sustain-side bus electrode 13d or scan-side bus electrode 13e has a width of 70 μm, while the sustain-side bus electrodes 13d or the scan-side bus electrodes 13e between vertically neighboring pixel cells are arranged at 70 μm intervals. Accordingly, the common bus electrode 57 can have a width of 210 μm.

This makes it possible to reduce the electrode resistance of the common bus electrode 57 to approximately 1/3 of that of the scan-side bus electrode 13e. In addition, the common bus electrode 57 may be increased in thickness from 1 through 9 μm, 5 μm on average as mentioned in the first embodiment, to 20 μm, thereby making it possible to reduce the resistance of the common bus electrode 57 to 1/12

of that of the scan-side bus electrode 13e.

This allows the voltage drop across the sustain-side bus electrode (the common bus electrode 57) to be further reduced from that of the sixteenth embodiment. This provides a reduced rate of reduction in the voltage applied to the sustain electrode 13a of each pixel cell. This provides a reduction in minimum voltage to be applied from outside during a light emission discharge and reduced spurious erases for discharging pixel cells, thereby providing more stabilized display operation. Incidentally, the maximum voltage remains unchanged which can be applied from outside without causing spurious discharges during a light emission discharge. This makes it possible to provide an increased operational voltage margin or the difference between the aforementioned maximum and minimum voltages.

Thus, it is made possible to set voltages with sufficient allowance with respect to a decrease in the aforementioned maximum voltage and an increase in the aforementioned minimum voltage caused by long-term operation. This allows the longevity of the plasma display panel to increase which is affected by spurious discharges or spurious erases, thereby making it possible to significantly improve the long-term reliability of the display device employing the plasma display panel.

In addition, the two neighboring sustain-side bus electrodes 13d are completely integrated with each other. This allows the common bus electrode 57 to have a width three to six times greater than that of the conventional

sustain-side bus electrode 13d. This makes it possible to increase the fabrication yield twice or more for a break in the electrodes. This effect is greater than that provided by the seventeenth embodiment in which the connecting portion 56 connects between the sustain-side bus electrodes 13d.

Incidentally, the display side of the bus electrode portion is formed in black. In this regard, with the scan-side bus electrode 13e being greatly different in shape from the common bus electrode 57 as in the eighteenth embodiment shown in Figs. 34 to 36, the configuration having intervals twice as large as the pitch of pixel cells would provide bad impression to the viewer. However, blackening between the neighboring scan-side bus electrodes 13e by means of the black horizontal barrier wall 23 would make it possible to eliminate the feeling of being apparently interfered.

Nineteenth embodiment

Now, a nineteenth embodiment according to the present invention is described below. Fig. 37 is a cross-sectional view illustrating a plasma display panel according to the nineteenth embodiment of the present invention. In the embodiment shown in Fig. 37, the thickness of the common bus electrode 57 and the scan-side bus electrode 13e, disposed across pixel cells adjacent to each other in the column direction, causes the surface of the insulating layer 18a to project by that thickness, thus creating the bumps 64 on the insulating layer 18a.

As described above, to raise the common bus electrode

57 and the scan-side bus electrode 13e to raise also the insulating layer 18a to form the bump 64 thereon, control may be exercised over the leveling property of the insulating layer paste upon being dried and the reflow property thereof upon being baked, by the material and adjustment of baking temperatures upon printing, drying, and baking the thick insulating layer 18a. For example, the amount of the thinner component of print paste is reduced to be less than usual and the maximum temperature of baking is also reduced by about 5 to 50℃, thereby making it possible to form such a bump 64. Furthermore, it is also effective to reduce the maximum temperature of baking and the length of time periods of the maximum temperature and temperatures before and after the maximum temperature.

This embodiment with the configuration described above can provide an effect equivalent to the horizontal barrier wall 23 without forming the horizontal barrier wall 23. This makes it possible to facilitate the fabrication process and provide a significant reduction in cost.

The common bus electrode 57 and the scan-side bus electrode 13e can have a thickness of 10 to 50 μm. Correspondingly, the bump 64 can have a height of 2 to 50 μm at the portions having no underlying bus electrodes 13d, 57. The bus electrodes 13d, 57 conventionally have a thickness of 1 to 9 μm and about 5 μm on average. In contrast, this embodiment provides the bus electrodes 13d, 57 with a thickness of 10 to 50 μm. Thus, this embodiment provides a second effect that the resistance of the scan-side bus

electrode 13e can be reduced to 1/2 to 1/10 of the conventional average electrode resistance.

Furthermore, the two neighboring sustain-side bus electrodes 13d are completely connected to each other to form the common bus electrode 57. It is therefore possible to reduce the electrode resistance of the common bus electrode to 1/6 to 1/30 of that of the two neighboring sustain-side bus electrodes 13d. This reduces the voltage drop across the sustain-side bus electrode 13d to be much less than that provided by the seventeenth embodiment. This provides a reduced rate of reduction in the voltage applied to the sustain electrode 13a of each pixel cell. This provides a reduction in minimum voltage to be applied from outside during a light emission discharge and reduced spurious erases for discharging pixel cells, thereby providing more stabilized display operation. Incidentally, the maximum voltage remains unchanged which can be applied from outside without causing spurious discharges during a light emission discharge. This makes it possible to provide an increased operational voltage margin or the difference between the aforementioned maximum and minimum voltages.

Thus, it is made possible to set voltages with sufficient allowance with respect to a decrease in the maximum voltage and an increase in the minimum voltage caused by long-term operation. This allows the longevity of the plasma display panel to increase which is affected by spurious discharges or spurious erases, thereby making it possible to significantly improve the long-term reliability

of the display device employing the plasma display panel.

Furthermore, the present invention allows the two sustain-side bus electrodes 13d, which are adjacent to each other in the prior-art configuration, to be completely integrated with each other, thereby making it possible to provide increased yield of fabrication for a break in the electrodes. This effect is greater than that provided by the seventeenth embodiment in which the connecting portion 56 connects between the sustain-side bus electrodes 13d.

<u>Twentieth embodiment</u>

Now, a twentieth embodiment according to the present invention is described below. Fig. 38 is a cross-sectional view illustrating a plasma display panel according to the twentieth embodiment of the present invention. This embodiment employs the common bus electrode 57 as the sustain-side bus electrode and is provided with two neighboring pairs of the scan electrode 13b and the scan-side bus electrode 13e, disposed overlapping with each other. As can be seen from Fig. 38, this allows the opening of pixel cells to be increased. This makes it possible to significantly increase the optical output efficiency and thereby dramatically reduce the power consumption of the plasma display panel. More specifically, for example, the luminous efficiency can be increased 1.3 times as high as that of the prior art. Using all this increase to reduce the power consumption makes it possible to reduce the light emission power by 30%.

<u>Twenty-first embodiment</u>

Now, a twenty-first embodiment according to the present invention is described below. Fig. 39 is a plan view illustrating a plasma display panel according to the twenty-first embodiment of the present invention. This embodiment allows the sustain electrode 13a to be narrowed at the root thereof for connecting to the sustain-side bus electrode 13d, thus providing the sustain electrode 13a with a narrowed portion 58. The common bus electrode 57, which commonly uses the electrodes disposed across two vertical pixel cells, may cause a spurious discharge to occur along the common bus electrode 57. However, this embodiment is provided with the narrowed portion 58, thereby making it possible to more positively prevent the spurious discharge transmitting along the common bus electrode 57, which commonly uses the electrodes disposed across two vertical pixel cells.

<u>Twenty-second embodiment</u>

Now, a twenty-second embodiment according to the present invention is described below. Fig. 40 is a plan view illustrating a plasma display panel according to the twenty-second embodiment of the present invention. In addition, to make the feature of this embodiment clear, shown in Fig. 41 is a plan view illustrating the configuration of pixel cells according to the eighth embodiment (see Figs. 20 to 22), from which this embodiment is originated. Referring to Figs. 41 and 40, a pixel cell centerline 59 is shown for comparison purposes. When Fig. 41 is compared with Fig. 40, Fig. 41 shows that the pixel

cell centerline 59 does not coincide with a centerline 60 of the discharge gap 22. This is because the scan electrode 13b and the sustain electrode 13a are provided with the same length of a long side 61 of the electrodes, the length being that of a substantial light-emitting portion, in accordance with the prior-art design technique by which the scan electrode 13b and the sustain electrode 13a are provided with the same area for discharging in pixel cells.

Experiments carried out by the present inventor show that this configuration provided by the prior-art design technique causes the discharge gap centerline 60, or the center of light emission, to be displaced from the pixel cell centerline 59 for defining the center of pixel cells to vary the centers of light emission at every two pixel cells in the vertical direction, thereby visualizing stripes having intensities that vary at pitch intervals twice as large as the vertical pixel cell pitch.

As shown in Fig. 40, to overcome this drawback, this embodiment provides the scan electrode 13b and the sustain electrode 13a with a change in length of the long side 61 of the electrodes, thereby allowing the pixel cell centerline 59 to coincide with the centerline 60 of the discharge gap 22.

In addition, by narrowing the root of the sustain electrode 13a as shown in Fig. 39, it is also possible to realize pixel cells arranged at the same intervals in the column direction and having generally the same distribution of light emission at the pixel cells.

With such an electrode arrangement, it is possible to effectively prevent the horizontal stripes from being viewed which have a repetitive pattern at twice pitch intervals.

Twenty-third embodiment

Now, a twenty-third embodiment according to the present invention is described below. Fig. 42 is a plan view illustrating a plasma display panel according to the twenty-third embodiment of the present invention. Fig. 43 is a cross-sectional view taken along line L-L of Fig. 42, and Fig. 44 is a cross-sectional view taken along line M-M of Fig. 42. In this embodiment, a black stripe pattern 62 (hereinafter referred to as the horizontal BS) is inserted in the row direction of Fig. 42. The horizontal BS 62 is provided on the first insulating substrate 11. The horizontal BS 62 is formed of an ordinary thick glass paste mixed with a black material (such as iron oxide or ruthenium oxide). The horizontal BS 62 being black acts to reduce the reflectivity of the display side and the surface reflectivity of the plasma display panel, thereby providing an effect of improving contrast.

In addition, suppose that white silver or the like having a high electrical conductivity is employed as the scan-side bus electrode 13e or the common bus electrode 57. Even in this case, the horizontal BS 62 is disposed so as to cover the bus electrodes 13e, 57, thereby providing a reduced surface reflectivity. For this reason, it is possible to use white silver electrodes of low resistance as the scan-side bus electrode 13e and the common bus electrode

57.

In the prior art, to reduce the reflectivity of bus electrodes formed of white silver, electrodes of black silver or the like were formed on the display side of the scan-side bus electrode 13e and the common bus electrode 57. However, the black silver is as expensive as the white silver and thus its drawback is the high cost of making electrodes. However, it is possible to reduce the cost by employing the comparatively inexpensive black BS 62 as in this embodiment.

Twenty-fourth embodiment

Now, a twenty-fourth embodiment according to the present invention is described below. Fig. 45 is a plan view illustrating a plasma display panel according to the twenty-fourth embodiment of the present invention. Fig. 46 is a cross-sectional view taken along line N-N of Fig. 45, and Fig. 47 is a cross-sectional view taken along line O-O of Fig. 46. This embodiment is the same as the twenty-third embodiment in having the black stripe pattern 62 formed in the horizontal direction but is different from the twenty-third embodiment in that horizontal BS's 62, each having the same width, are disposed at the same intervals to be vertically symmetric at each pixel cell. With the highly reflective scan-side bus electrodes 13e and common bus electrodes 57 being effectively covered, this makes it also possible to prevent horizontal fringes occurring in the column direction (the vertical direction) of Fig. 45 at pitch intervals twice as great as the pixel cell pitch.

Twenty-fifth embodiment

Now, a twenty-fifth embodiment according to the present invention is described below. Fig. 48 is a plan view illustrating a plasma display panel according to the twenty-fifth embodiment of the present invention. Fig. 49 is a cross-sectional view taken along line P-P of Fig. 48, and Fig. 50 is a cross-sectional view taken along line Q-Q of Fig. 48. This embodiment is the same as the twenty-third embodiment in having the black stripe pattern 62 formed in the horizontal direction but is different from the twenty-third embodiment in that the horizontal BS 62 of this embodiment is disposed between the scan-side bus electrodes 13e to overlap therewith.

The horizontal BS 62, a horizontal stripe formed of two neighboring black or gray scan-side bus electrodes 13e, and a horizontal stripe formed of a black or gray sustain-side bus electrode 13d are adapted to have the same width and all the horizontal stripes are disposed at the same intervals. This makes it possible to prevent horizontal fringes occurring in the vertical direction at pitch intervals twice as great as the pixel cell pitch. With the entire display side being formed in black, the scan-side bus electrode 13e and the common bus electrode 57 provide an effect of further enhancing contrast.

Twenty-sixth embodiment

Now, a twenty-sixth embodiment according to the present invention is described below. Fig. 51 is a plan view illustrating a plasma display panel according to the

twenty-sixth embodiment of the present invention. Fig. 52 is a cross-sectional view taken along line R-R of Fig. 51, and Fig. 53 is a cross-sectional view taken along line S-S of Fig. 51. The basic configuration of Figs. 51 to 53 is the same as those of the twenty-third and the twenty-fourth embodiments but is different therefrom in that the horizontal BS 62 is disposed on top of the transparent scan electrode 13b and the sustain electrode 13a. With this arrangement, the horizontal BS 62 having a thickness of 1 to 5μm is to be formed on top of the transparent scan electrode 13b and sustain electrode 13a, which are normally formed to have a thickness of about 0.2μm.

Forming the scan electrode 13b and the sustain electrode 13a, which are thinner by 1/5 or more than the horizontal BS 62, on the horizontal BS 62 would cause a break in the scan electrode 13b and the sustain electrode 13a to be apt to occur due to the stepped portion at the edge of the horizontal BS 62. However, with the arrangement described above, this break can be effectively prevented. In this case, it is necessary to ensure the electrical connection between the scan electrode 13b and the scan-side bus electrode 13e or between the sustain electrode 13a and the common bus electrode 57. To this end, it is effective to increase the diameter of particles of the material for use with the horizontal BS 62 to make the structure of the horizontal BS 62 porous, thereby ensuring the electrical connection between the scan electrode 13b and the scan-side bus electrode 13e or between the sustain electrode 13a and

the common bus electrode 57.

Alternatively, as shown in a modified example of this embodiment of Fig. 54, it is effective to ensure the connection between the scan electrode 13b and the scan-side bus electrode 13e or between the sustain electrode 13a and the common bus electrode 57. Incidentally, Fig. 54 shows a window portion 63, however, this portion may be notched. In all the embodiments described above, the configuration of bus electrodes has not been mentioned. However, as in the prior art, the bus electrode, when illuminated, makes it possible to reduce reflectivity with the display side being formed of black metal electrodes and the inside of pixel cells being formed of metal electrodes, having a low resistance, of a given color.

The aforementioned embodiments are adapted to be driven by the same method as that of the prior art, allowing each pixel cell to have an independent scan electrode and pixel cells adjacent to each other in the column direction (the vertical direction) to share a common electrode. However, the present invention is intended to specify the structure of pixel cells of a plasma display panel but not intended to specify how to use each electrode. Thus, as a matter of course, the scan electrode described above with reference to the foregoing embodiments may be used as the sustain electrode and the sustain electrode may also be used as the scan electrode. An example of a driving method for this case is explained briefly below.

Fig. 55 is a schematic view of the arrangement of

electrodes of a plasma display panel, illustrated to explain how to apply a driving method different from those of the prior art to the plasma display panel having the structure of pixel cells according to the present invention described above. Referring to Fig. 55, reference symbol 113b denotes scan electrodes, 113a denotes sustain electrodes, and 14 denotes column electrodes. The scan electrode 13b described with reference to the first to twenty-fifth embodiments is used as the sustain electrode 113a, and the sustain electrode 13a is used as the scan electrode 113b.

Pixel cells 20 are defined at the intersections of a pair of scan electrodes 113b and a sustain electrode 113a, parallel to one another, and the column electrodes 14 orthogonal thereto. Vertically neighboring pixel cells 20 share the scan electrodes 113b, which are in turn coupled to the output pin of a scan driver IC (not shown).
With this arrangement, the number of outputs of the scan driver IC is one-half of that of the display lines. The sustain electrodes 113a are divided into a first sustain electrode group 103a located above the scan electrodes 113b and a second sustain electrode group 103b located below the scan electrodes 113b. Electrical connection (not shown) is provided for each of the groups outside the panel or outside the display area within the panel.

Fig. 56 is a cross-sectional view taken along the column electrode 14 of Fig. 55. Fig. 56 is a cross-sectional view illustrating the main portion of the plasma display panel corresponding to Fig. 55, also corresponding

to Fig. 8 of the first embodiment. Fig. 56 is different from Fig. 8 in that the scan electrode 13b and the sustain electrode 113a are interchanged, and the scan-side bus electrode 13e and sustain-side bus electrode 113d are interchanged.

Fig. 57 is a timing chart illustrating this drive method. In addition, Figs. 58A to 58D are schematic views of the state of wall charges inside the pixel cells of the panel shown in cross section in Fig. 56, each illustrating the state of wall charges at the end of each cycle of sub-fields A to D in Fig. 57.

The operation by the driving method is explained below with reference to Fig. 57 and Figs. 58A to 58D. First, during the first preliminary discharge cycle A, a negative sawtooth preliminary discharge pulse Vpc is applied to the sustain electrode group 103a. In phase therewith, a preliminary discharge pulse Vps having the reversed polarity is applied to the scan electrode 113b. The voltage difference attained by a preliminary discharge pulse Vp between the scan electrode 113b and the sustain electrode 113a is set to be higher than a discharge initiating voltage between the sustain electrode 113a and the scan electrode 113b. In addition, the same waveform voltage as that for the scan electrode 113b is applied to the sustain electrode group 103b. In the pixel cell 20a including the sustain electrode group 103a, a discharge occurs at the time at which the discharge initiating voltage has been exceeded during the application of the preliminary discharge pulse Vp,

with the scan electrode 113b being positive. This causes negative wall charges to build up on the scan electrode 113b and positive wall charges to build up on the sustain electrode 113a. At this time, in the pixel cell 20b including the sustain electrode group 103b, no voltage difference is established and therefore no discharge occurs.

Then, during the first select operation cycle B, a scan pulse Vw is applied to the scan electrode 113b and a data pulse Vd is applied to the column electrode 14 in response to display data. This causes the wall charges to vanish only in the pixel cell 20 to which the data pulse Vd has been applied. Furthermore, a first sustain discharge pulse Vs11 is applied to the scan electrode 113b to cause a discharge to occur only at the pixel cell 20a having wall charges built up or in the "ON" state. At the same time, wall charges of reversed polarities are built up on the scan electrode 113b and the sustain electrode 113a, respectively. Fig. 58 illustrates the case where the pixel cell 20a is in the "ON" state.

Likewise, during the subsequent second preliminary discharge cycle C and second select operation cycle D, a selective operation is carried out only in the pixel cell 20b including the sustain electrode group 103b to cause wall charges to build up only in the pixel cell 20b that is in the "ON" state. Fig. 58D illustrates the case where the pixel cell 20b is in the "ON" state. Even in this case, no change occurs in the pixel cell 20a including the sustain electrode group 103a.

Then, during the sustain cycle E, a discharge sustain pulse Vs having a reversed polarity is applied to all the scan electrodes 113b and sustain electrodes 113a, thereby causing a discharge only in the pixel cells 20, where the wall charges have not been erased, to obtain light emission for display purposes during the select operation cycles B and D. Furthermore, during the sustain erase cycle F, a blunt-waveform sustain erase pulse Ve is applied to erase wall charges to thereby terminate the discharge, and then operation proceeds to the subsequent sub-field. By the foregoing operations, it is possible to perform the "ON" and "OFF" control on all the pixel cells 20 within one sub-field.

As described above, it is also possible to perform the light-emitting and non-light-emitting control on each pixel cell by allowing pixel cells adjacent to each other in the vertical direction to share a scan electrode and using an independent sustain electrode for each pixel cell.

Furthermore, in each of the aforementioned embodiments, the scan electrode and the sustain electrode are completely cut apart in the row direction and each pixel cell is provided with a separate scan electrode 13b and sustain electrode 13a. However, the effects of the present invention can be obtained even by the scan electrode 13b and the sustain electrode 13a which are provided with a notched portion between pixel cells 20 adjacent to each other in the row direction and thus not completely separated from each other.